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UTILITY SERIAL NUMBER 08/533,207		PATENT DATE DEC 01 1998		PATENT NUMBER	
SERIAL NUMBER 08/533,207	FILING DATE 09/25/95	CLASS 109	SUBCLASS 620	GROUP ART UNIT 2503 2722	EXAMINER PRENTY
APPLICANTS KEIICHIRO KATA, TOKYO, JAPAN; SHINICHI CHIKAKI, TOKYO, JAPAN.					
CONTINUING DATA*** VERIFIED MP None					
FOREIGN/PCT APPLICATIONS*** VERIFIED JAPAN 237653/1994 09/30/94 MP					
Foreign priority claimed 35 USC 119 conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> yes <input type="checkbox"/> no					
Verified and Acknowledged <input checked="" type="checkbox"/> MP		AS FILED <input checked="" type="checkbox"/>	STATE OR COUNTRY JPX	SHEETS DRWGS. 4	TOTAL CLAIMS 502
Examiner's Initials			INDEP. CLAIMS 257	FILING FEE RECEIVED \$401.00	ATTORNEY'S DOCKET NO. WN-14391-0-P
ADDRESS WHITHAM CURTIS WHITHAM & MCGINN RESTON INTERNATIONAL CENTER SUITE 900 11800 SUNRISE VALLEY DRIVE RESTON VA 20191					
TITLE PROCESS FOR MANUFACTURING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR WAFER					

U.S. DEPT. OF COMM./PAT. & TM--PTO-436L (Rev. 12-94)

PARTS OF APPLICATION FILED SEPARATELY		7-22-98	
NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
7-21-98		Total Claims 12	
ISSUE FEE		Print Claim 1	
Amount Due 1300.00	Date Paid 7-22-98	DRAWING	
Label Area		Sheets Drwg 4	
		Figs. Drwg 20	
		Print Fig 40	
		ISSUE BATCH NUMBER G78	
PREPARED FOR ISSUE			
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